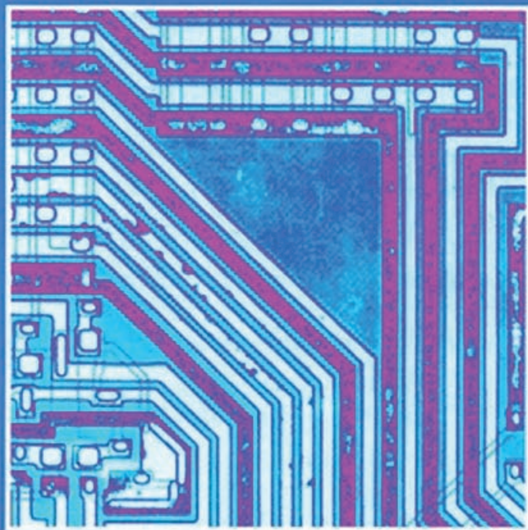
Silicon Devices

Structures and Processing

Edited by Kenneth A. Jackson



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Silicon Devices

Structures and Processing

Edited by
Kenneth A. Jackson

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Preface

This volume covers the basic processes involved in the manufacture of silicon devices, starting with purification and crystal growth, includes a description of various device structures, and concludes with a description of the processes involved in device fabrication. The chapters are drawn from the book "Semiconductor Processing" which is Volume 16 of the VCH series on Materials Science and Technology.

It may be surprising to some how little the descriptions of the processing depends on the fundamental physics of semiconductors. The properties of the silicon determine what is to be done in the manufacturing process, but not how it is to be done. The processing depends critically on the properties of the wide variety of materials which are used, and the processing in a semiconductor fabrication facility, a "fab", is a complex multi-stage sequence. The cost of a new fab, which is now at the incredible level of about one billion US dollars, is a measure complexity of the processing and of the sophistication of the equipment used.

Semiconductor processing often makes use of materials at a limit of their capability. The silicon crystals used as starting material are as pure and as perfect as single crystals can be made, deposited layers are uniform and defect free, conductor cross-sections are limited by current densities, insulating layers must be uniform in thickness and free of pinholes. Ultra-purity is required not only of the silicon, but also of all the processing chemicals such as dopants, etchants, and cleaning materials, including the water. Even the air in a semiconductor fab is special: a whole technology exists to build clean rooms which are designed to limit the number and size of airborne particulates. All of the processing materials and processes have been and are continually scrutinized in minute detail to improve their efficiency and performance, and to reduce costs.

This volume does not deal with the semiconductor design process, although design is clearly the essential first step in the production of a device. The design of new processors, memory chips and ASICs (Application Specific Integrated Circuits) is now implemented with extensive use of computer aided design. The electrical circuits are designed using computers and the designs are tested by computer simulation. The layout of the circuit components based on the circuit design is done by a computer which prepares the input for an electron beam writer which writes a mask set. The mask set is delivered to the fab where the masks are used successively to pattern the distribution of various dopants in the semiconductor, to pattern the dielectric layers and the conductor metallizations. Many circuit designers have never been in a fab, and the people who work in fabs need to know little about the design process. The other major aspect of semiconductor manufacture which is not dealt with in this volume is testing. Simple circuits are sample tested, but expensive chips such as microprocessors are subject to extensive electrical and performance testing. Testing all of the transistors on a chip which has ten million transistors and only a few hundred input/output pins requires a complex test procedure. The test stations are expensive and the tests are time consuming, so that testing is a major cost factor in semiconductor production.

This volume deals with the basic manufacturing processes for silicon. The fabrication process starts with the purification of the silicon followed by the growth of single crystals. The crystals are sliced into wafers which are then polished, so that silicon arrives at the fab as polished wafers. Each wafer diameter requires its own suite of processing equipment, and at the present time wafers up to twelve inches in diameter are being processed. Crystal growth and wafering processes for silicon are discussed by J. G. Wilkes in first chapter. Device structures including potential-effect devices, field-effect devices, quantum-effect devices, microwave devices and photodetectors are described in the second chapter by C.-Y. Chang and S. M. Sze. In the concluding chapter, D.-L. Kwong discusses device processing, including gettering, device isolation, dielectrics, junction formation, metallization, and cluster tool technology. The processing of a wafer typically involves hundreds of separate steps, but several hundred chips can be made from a single wafer. There is a continuing trend to use larger wafers and finer features on the wafers in order to get more chips from each wafer.

There are several important aspects of the fabrication of semiconductors which are beyond the scope of this volume. These include photolithography, which is used for the patterning of the dopants to make the devices, as well as the dielectrics and metallization. The feature size on wafers is now at the limit of optical resolution. The very sophisticated chemistry is needed to design the photosensitive materials which are used is beyond the scope of this volume. Similarly, the ion implantation process which is used for the selective introduction of dopants into the semiconductor is not discussed in detail, nor is the packaging technology used to protect the chips and to connect them to the outside world.

Silicon processing technology is very advanced in scale of integration and so, if a semiconductor device can be made with silicon, it will be. Silicon is used almost exclusively for logic and memory devices, and although it is used for photodetectors and solar cells, it cannot be used to make devices which emit light, such as light emitting diodes (LED's) or semiconductor lasers. Semiconductor light source devices are the domain of compound semiconductors, such as GaAs, which are discussed in a companion volume. Although there are many aspects of the processing which are common to both silicon and compound semiconductors, many of the devices are different, and the basic chemistry of the materials introduces significant differences in processing.

I would like to thank the authors who have taken time from their very busy schedules to prepare their chapters. They are experts in processing technology because they are involved with it on a daily basis, and it has been difficult for many of them to find the time to write. But the result is a valuable and timely description of the state-of-the art for silicon processing.

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Tucson, AZ
August, 1998

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List of Symbols and Abbreviations

A_n	Fourier series coefficient
a_0	lattice constant (for Si, $a_0 = 5.42$ Å)
A_0	constant
B	slice bow depth
C	concentration
C_H	crystal habit
C_l	concentration in liquid
C_p	concentration (of oxygen in oxide) in particle
C_s	concentration in solid
C_{es}	equilibrium solid solubility concentration
C_0	initial concentration
d	diameter
D	diffusion coefficient
E_c	activation energy for the formation of a particle of critical radius
f_t	cut-off frequency
$\bar{f}_t$	mean value of f_t
ΔF_v	volume free energy change of a precipitate
F_x, F_y, F_z	magnitudes of the forces generated at the edge during sawing
g	fraction of melt solidified
h	height
ΔH	enthalpy of reaction
$I(\theta)$	detector signal
I	interstitial
I_{cb}	collector–base current
k	Boltzmann constant
k_{eff}	effective distribution coefficient
k_0	equilibrium distribution coefficient
N	number of particles
N_c	number of particles of critical radius
$\mathrm{n_f}$, $\mathrm{n_t}$	fast neutron, thermal neutron
n_1	number of oxygen atoms in axial bonds
n_2	number of oxygen atoms in other bonds
$[\mathrm{O_i}]$	bound interstitial oxygen concentration
Pr	Prandtl number
r	radius
R	radius of the total volume from which oxygen condenses into a precipitate
r_c	critical radius
r_0	radius of a final precipitate particle, small compared with R
t	time
T	absolute temperature
T_m	melting point (Si: 1412 °C)
$t_{1/2}$	half life of radioactive species
t_{Si}	thickness of a silicon slice

ΔT temperature difference
v velocity
V vacancy
v_g velocity of growth
W_c intrinsic X-ray signal half width
W_m measured X-ray signal half width
ΔW rocking curve broadening

α alpha particle
$\alpha_{\|}$ absorption coefficient for polarized infrared light parallel to the stress axis
$\alpha_{\perp}$ absorption coefficient for polarized infrared light perpendicular to the stress axis
γ gamma particle
δ boundary layer thickness
ε strain
θ test sample angle
θ_B Bragg angle, X-ray reflection
λ_n Fourier coefficient (with dimensions of inverse length)
λ_0 constant
ν kinematic viscosity
σ surface free energy
τ relaxation time
τ_n, τ_0, τ_* relaxation time constants
ω angular velocity

AC alternating current
ACR advanced carbothermic reduction
ASTM American Society for Testing Materials
BP boiling point
CMOS complementary, using both n- and p-type, metal–oxide–silicon device
CVD chemical vapor deposition
CZ Czochralski material
DC direct current
DCS dichlorosilane
DI deionized
DRAM dynamic random access memory
EBE extended bulk epitaxy
EG enhanced gettering
FZ float zoned (material)
HF high frequency
HI–LO high temperature–low temperature (heat treatment)
LPCVD low pressure chemical vapor deposition
MG-Si metallurgical-grade silicon
MOS metal–oxide–silicon (device) (n-MOS, p-MOS refer to the dopant type structure employed)

NFZ	nitrogen-doped float zone (material)
NTD	neutron transmutation doping
NTP	normal temperature and pressure
ppba	atomic parts per billion (10^9)
ppma	atomic parts per million
ppt	parts per trillion (10^{12})
psi	pounds per square inch
RF	radio frequency
rpm	rotations per minute
SANS	small angle neutron scattering
SIMS	secondary ion mass spectrometry
SRAM	static random access memory
TCS	trichlorosilane
TD	thermal donor
TIR	total integrated reading (of bow or warp)
UHF	ultrahigh frequency
ULSI	ultra large scale integration
UV	ultraviolet
VLSI	very large scale integration
WCA	water classified alumina

1.1 Introduction

Silicon today is a commodity, its price subject to all the forces of supply and demand in an intensely competitive market, and this has driven the development of high yield processes for the tight tolerance materials demanded. While discrete and power device manufacture calls for some float zoned, and neutron transmutation doped (NTD) silicon; the worldwide compass of integrated circuit manufacture consumes more than 75% of all the semiconductor silicon produced. The development of the product market distribution is shown in Fig. 1-1. Supply of this material is dominated by Czochralski crystal growth, the operational scale of which has increased from charges weighing a few hundred grams, around 1962, to the current units of 60 kilogram and more.

The evolution of the semiconductor industry as we now know it began in the 1950s, when many of the then large electrical companies became involved in the chemistry and metallurgy of Germanium. Their starting point was GeO_2, the dioxide, which had to be reduced to metal powder, melted, zone refined, and crystals grown, before the machining operations which led to discrete devices. Germanium being an expensive rare element, the machining itself generated valuable byproduct sludges which had to be recovered. The extreme purity necessary led into problems in chemical and physical analysis, materials of containment, and in general chemical engineering.

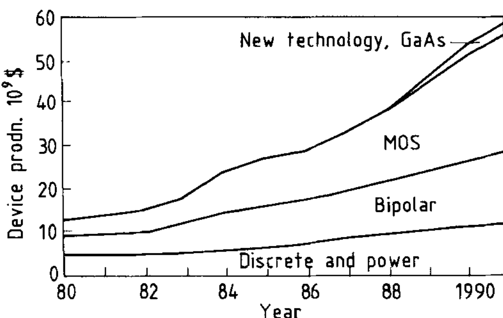


Figure 1-1. Development of the semiconductor product market.

In retrospect, very few of these electrical companies possessed either the resources or the experience needed for such work; so when, only shortly afterwards, silicon was introduced, almost all of them took the opportunity to withdraw from the chemical end of the business. Silicon is one of the most abundant elements, and so the sludges are of no economic importance. Henceforth their starting point became the ultrapure polycrystalline silicon from which they made their own single crystal. With time, the number of companies doing even this has steadily declined, until today few of the electronics manufacturers have any involvement in bulk material processing. Indeed most purchase polished slices, cleaned and packaged, furnace ready, for fabrication lines. A number of the device makers still carry out epitaxy and, to that extent alone, retain a residual materials activity.

In modern very large scale integration (VLSI) circuits, lithographic feature sizes have been reduced to 1 µm or less, and use multilevel interconnects to enable the production of high complexity devices of steadily rising chip area. Consequently, as the number of chips per wafer decreases, so there has been an accompanying call for ever larger wafer diameter – to reduce perimeter wastage, and to improve fabrication line yield and throughput, as shown in Fig. 1-2 – hence the continuous need to scale up crystal size, this demanding extremely heavy investment.

This scaling has not been at the expense of quality – in fact quite the reverse. As more has been learnt about the relation-

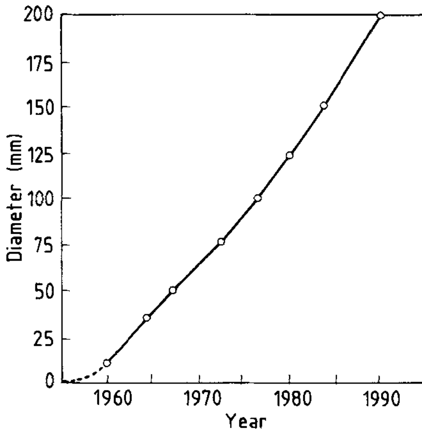


Figure 1-2. The year of introduction of the largest silicon wafers in production. (Note: This trend continues. A very small number of companies, mainly Far East, are now looking at 250 mm diameter possibilities.)

ship between materials properties and the device parameters, so the demand for better performance from the silicon has grown. If one compares a typical purchasing specification of even the mid 1970s, with that in force today for a similar application endproduct, the increase in the number of parameters specified, and the narrowing of virtually all tolerances, is marked. Contributory factors leading to this position include: Fine geometry lithography, needing slices of a flatness not even contemplated ten years ago; cassette, and now robotic, handling techniques, which call for close machining tolerances, and edge rounded slices, to prevent chipping and particles accumulating in ultraclean fabrication equipment. Research into the behavior of oxygen and carbon precipitation in bulk silicon under device furnacing conditions has led to the introduction of new specification parameters, new crystal processing methods, and to the concept of "crystal engineering". Controlled oxide precipitation in slices is carried out, prior to their use in fabrication lines, to provide sites for the intrinsic gettering of unwanted fast diffusing electrically deleterious impurities, away from the surface layer where the MOS devices are made. Residual mechanical damage sites after the crystal machining provide similar extrinsic gettering sites. For many applications in "crystal engineering" today, combinations of controlled mechanical and oxide precipitate gettering are used together to achieve optimum performance from the silicon, to match the particular device requirements in MOS, CMOS, and bipolar configurations. To achieve this matching it is necessary to examine the total thermal inventory of the multistage fabrication process, in order to select the most appropriate structure.

While the early 1990s have seen a general slowdown in world economies, the surge in the personal computer market, linked to the major developments in microprocessor chips, has meant that device production revenues have continued to grow, by 1993, to $ 60-70 billion (10^9), and are projected to be in the range $150-200 billion by the year 2000. These microprocessor chips are of ever increasing size and complexity; for example the Intel Pentium with around 3 million transistors, running at a speed of 100 million instructions per second, is about 0.5 sq. in. ($\sim 3\ cm^2$) in area. In memory chips the 16 Mbit DRAM is being followed by the 256 Mbit version, and since each DRAM cell needs one transistor, even with shrinking all dimensions the chip size is increasing. Charge coupled devices for displays also require large-area chips. Such ultra large scale integration (ULSI) applications today are leading the demand for Czochralski silicon wafers with diameters of 200 mm (8″), and inevitably still bigger will follow. For these diameters, the current pullers have to be scaled up

further towards 100–150 kg machines. The larger thermal masses will impose difficulties in the control and uniformity of the dopant, oxygen, and crystal defect concentrations. Finer dimension lithography needs ultra flat wafers, and particulate contamination levels of less than 10 particles greater than 0.1 μm per wafer are expected. Leakage control in large DRAMs requires metallic surface contamination to below 10^9 atoms/cm. These are severe challenges at the final wafer cleaning and packaging stages.

Overall, larger slices, made to extremely close tolerances by rigidly defined processing, from silicon that conforms to tightly specified criteria with respect to uniformity, dopants, impurities, point defect precipitates, clean surface characteristics, and metrology, are required of the materials vendors. Yet as the market competition is fierce, all of this is wanted at the minimum possible price – a constraint that reflects back through every step in silicon material manufacture. Thus right back in the raw material sector, over the past twenty years the supply of silicon has steadily become concentrated into fewer large specialist merchant vendors, and usually these operate as a division within some much bigger general chemical corporation. Many of the same companies are now involved in the present ruthless shakeout of the parallel gallium arsenide material market, as this sector, in the 1990s, is becoming commercially more significant. Thus the highly competitive commodity environment, which can never be ignored, is the constant background influence against which this chapter is set.

1.2 Metallurgical-Grade Silicon

The source of the raw silicon used for semiconductor purposes is metallurgical-grade silicon, manufactured by the carbothermic reduction of silica in an electric arc furnace. Silica, occurring naturally as quartzite, in vein quartz, and in sandstone, and as unconsolidated sands and gravels, is a common mineral with worldwide distribution. Silicon, after oxygen, is the second most abundant element, but does not occur naturally in its elemental form. Silica, either free as in quartz or in the many forms of silicate igneous rocks, constitutes about a quarter of the earth's crust. However, the silicon metal producers demand an ore purity of better than 99% SiO_2, and also place tight restrictions on the allowable concentrations of various impurities present – in particular arsenic, phosphorus, and sulfur – so that often only a small fraction of an ore deposit meets their purity specification. Geologically washed out gravel from river bed deposits, and similarly leached out quartz sands, are a source of very high purity silica. Vast new deposits, yielding quartzite ore of the highest purity available today, have been discovered in Arkansas, U.S.A., from which monocrystals weighing several tons apiece have been displayed in exhibitions worldwide.

In the traditional electric arc furnace process, which has been used for most of this century, chunky quartzite is reacted with carbon, as the reductant, in the forms of coal, coke, or charcoal, which can be a source of at least an order of magnitude greater impurity levels than present in the silica. The overall reaction appears simple:

$$SiO_2 + 2C \rightarrow Si + 2CO \quad (1)$$

However, as discussed by Healy (1970), the actual reaction sequence in the different temperature zones of the furnace is far more complex than this, as set out in the schematic diagram of Fig. 1-3.

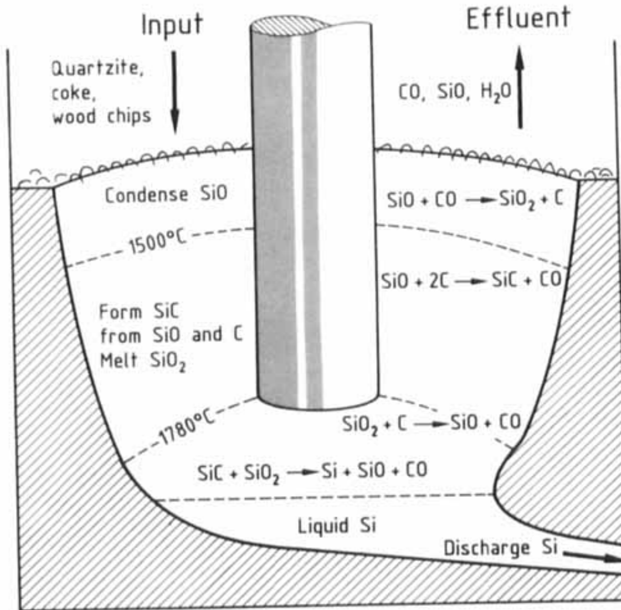
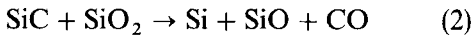


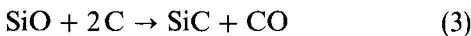
Figure 1-3. Schematic diagram of the submerged-electrode electric arc furnace for the production of metallurgical grade silicon.

(a) Towards the bottom of the furnace, in the region of the arc between the electrodes where the temperature can exceed 2000 °C, silicon is produced by the reaction



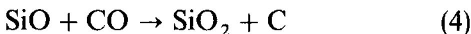
$$SiC + SiO_2 \rightarrow Si + SiO + CO \qquad (2)$$

(b) Above this, at a somewhat lower temperature, around 1700–1500 °C, the rising byproduct gases react to form the intermediate product silicon carbide by



$$SiO + 2\,C \rightarrow SiC + CO \qquad (3)$$

(c) Nearer to the top, where the temperature falls below 1500 °C, as is expected thermodynamically, the reverse reaction predominates:



$$SiO + CO \rightarrow SiO_2 + C \qquad (4)$$

The input materials are fed into the top of the furnace, while liquid silicon is periodically tapped from the bottom and cast into ingots. If this casting is carried out directionally, under the conditions referred to as normal freezing, impurity redistribution can be used to effect some purification, following the well equation by Pfann (1952, 1958):

$$C_s = k_{eff}\, C_0 (1 - g)^{(k_{eff} - 1)} \qquad (1\text{-}1)$$

For the arc process to run properly, it is essential to maintain porosity throughout the charge to allow uniform SiO and CO gas flow, and to permit the escape of CO, some SiO, and H_2O from the top. To assist this wood chips may be included in the feedstock, and the silica must be of a form which does not readily crumble during initial heating in the upper part of the furnace, which could lead to premature fusion and crusting over, with the risk of a dangerous pressure buildup within the charge. Clearly the carbothermic reduction of silica is not a trivial process.

Crossman and Baker (1977) have given a very interesting comparison of the impurities present in typical quartzite and the carbon used, related to the spectrographic analysis of more than 2000 tons of the met-

allurgical-grade silicon produced. Their data, collected into Table 1-1, indicated total impurity levels in the quartzite of around 750 ppma; in the carbon 8000 ppma, and in the resulting metallurgical-grade silicon (MG-Si) 4000–4500 ppma. Within this analysis the two predominant impurities are seen to be aluminum and iron, largely originating from the carbon, and taken together accounting for over 80% of that in the silicon product. Since these results referred to MG-Si to be used for the production of semiconductor grade polycrystal silicon, the importance of the purity of the carbon source is underlined.

Recent developments have focused on improved and cleaner processes, better quality carbon, and efforts to develop quartz sands as an alternative low cost and high purity source. Maintaining charge porosity constitutes the most serious restriction in the operation of the submerged arc furnace, and much attention has been focused on how to meet, or circumvent this problem. In work aimed to reduce drastically the impurities in arc furnace silicon, Dosaj et al. (1978) working at Hemlock Semiconductor Corp. U.S.A. reported using a high purity silica source together with carbon black powder, pelletized with pure sucrose binder, to obtain MG-Si at 99.99% purity. Although the boron content of the material was relatively low, this particular element tends to be more persistent through the later stages of semiconductor silicon manufacture, and therefore recently there has been interest in exploiting the lower boron content of carbon obtained from petrocoke.

Table 1-1. Impurities in silica, carbon, and metallurgical-grade silicon.

Impurity	Quartzite (ppma)	Carbon[a] (ppma)	MG-silicon[b] (ppma)
Al	620	5500	1570 ± 580
B	14	40	44 ± 13
Cr	5	14	137 ± 75
Fe	75	1700	2070 ± 510
P	10	140	28 ± 6
Others	10	600	—
Mn			70 ± 20
Ni			47 ± 28
Ti			163 ± 34
V			100 ± 47

[a] Weighted; [b] average value ± standard deviation.

The pelletization of upgraded quartz sands can provide very pure silica in a suitable form. This material then has to be agglomerated to lumps, either separately or mixed with carbon powder. This approach has been studied by several groups, including Elkem A/S, Norway, the largest European silicon metal producer, but until now it has only been taken to a development stage. The Siemens advanced carbothermic reduction (ACR) process has recently been described by Aulich et al. (1985), in which high purity pelletized quartz sand is reduced by carbon granules, prepared from carbon black briquettes, which had been leached with hot HCl to a purity comparable to that of the silica. Since in an arc furnace about 10% of the carbon comes from the electrode, the effective carbon impurity level was somewhat higher. Nevertheless a substantial overall impurity reduction was achieved.

A more radical approach to overcoming the porosity problem has been the application of DC plasma-arc techniques to the production of ferrosilicon alloys and silicon metal. The most important feature of the plasma-arc furnace here is that it can process ore fines directly, without prior briquetting or pelletization. The potential of this route is supported by the extremely efficient plasma purification of normal MG-Si, by factors of up to 100 000, re-